Not Recommended for new Designs

UNITRODE

bq4017/bq4017Y

2048Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Conventional SRAM operation; unlimited write cycles
- 5-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4017 is a nonvolatile 16,777,216-bit static RAM organized as 2,097,152 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

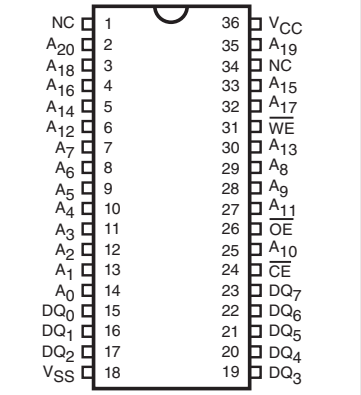
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4017 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4017 has the same interface as industry-standard SRAMs and requires no external circuitry.

Pin Connections



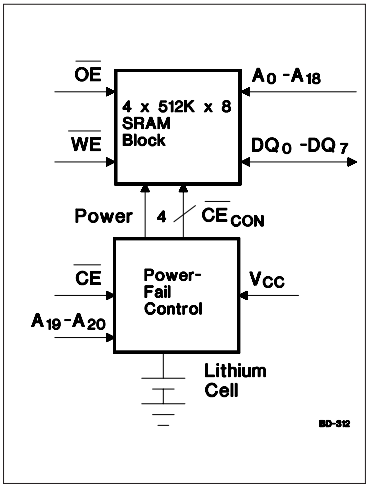
36-Pin DIP Module

PN401701.eps

Pin Names

A_0–A_{20}	Address inputs
DQ_0–DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	Supply voltage input
V_{SS}	Ground
NC	No connect

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4017MC -70	70	-5%	bq4017YMC -70	70	-10%

5/95

Not Recommended for new Designs

Functional Description

When power is valid, the bq4017 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4017 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4017 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4017Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4017 have an extremely long shelf life. The bq4017 provides data retention for more than 5 years in the absence of system power.

As shipped from Unitrode, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC}$ + 0.3
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Not Recommended for new Designs

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4017Y
		4.75	5.0	5.5	V	bq4017
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CC}min \leq V_{CC} \leq V_{CC}max$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 4	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 4	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	7	17	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$0V \leq V_{IN} \leq 0.2V$, $\overline{CE} \geq V_{CC}$ - 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2
I_{CC}	Operating supply current	-	75	115	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$,$I_{I/O}$ = 0mA, A19 < V_{IL} or A19 > V_{IH}, A20 < V_{IL} or A20 > V_{IH}
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4017
		4.30	4.37	4.50	V	bq4017Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Not Recommended for new Designs

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	40	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	40	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

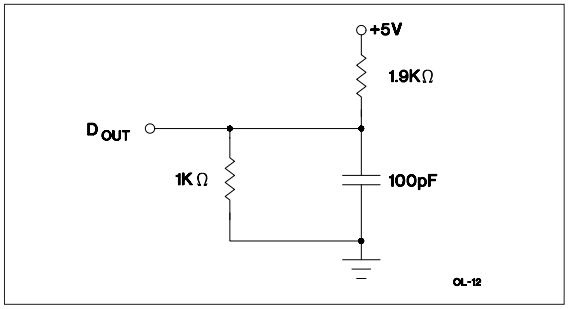


Figure 1. Output Load A

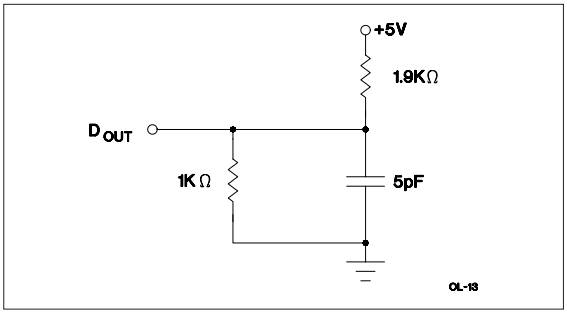


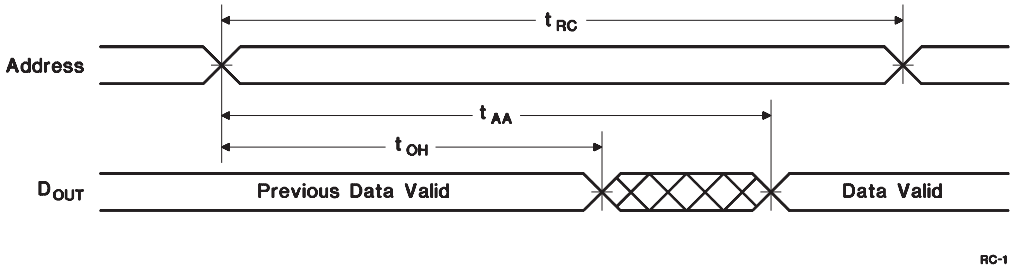
Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

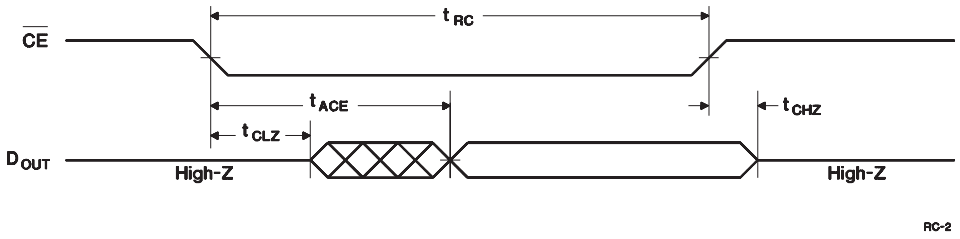
Symbol	Parameter	-70		Unit	Conditions
		Min.	Max.		
t_{RC}	Read cycle time	70	-	ns	
t_{AA}	Address access time	-	70	ns	Output load A
t_{ACE}	Chip enable access time	-	70	ns	Output load A
t_{OE}	Output enable to output valid	-	35	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

Not Recommended for new Designs

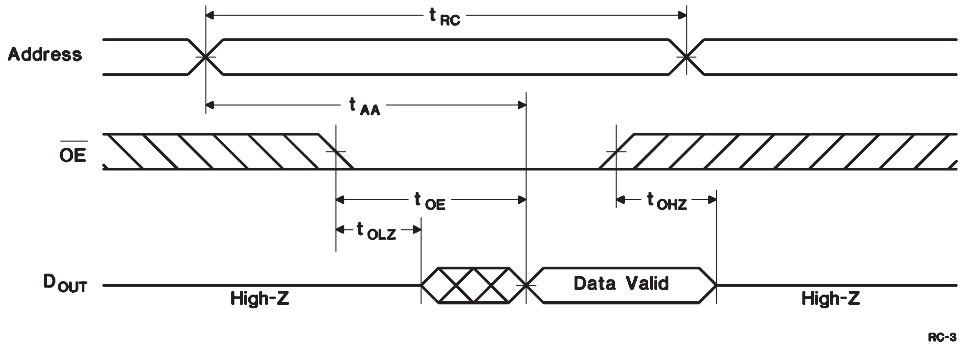
Read Cycle No. 1 (Address Access)[1,2]



Read Cycle No. 2 (CE Access) [1,3,4]



Read Cycle No. 3 (OE Access) [1,5]



Notes:

1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

Not Recommended for new Designs

Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

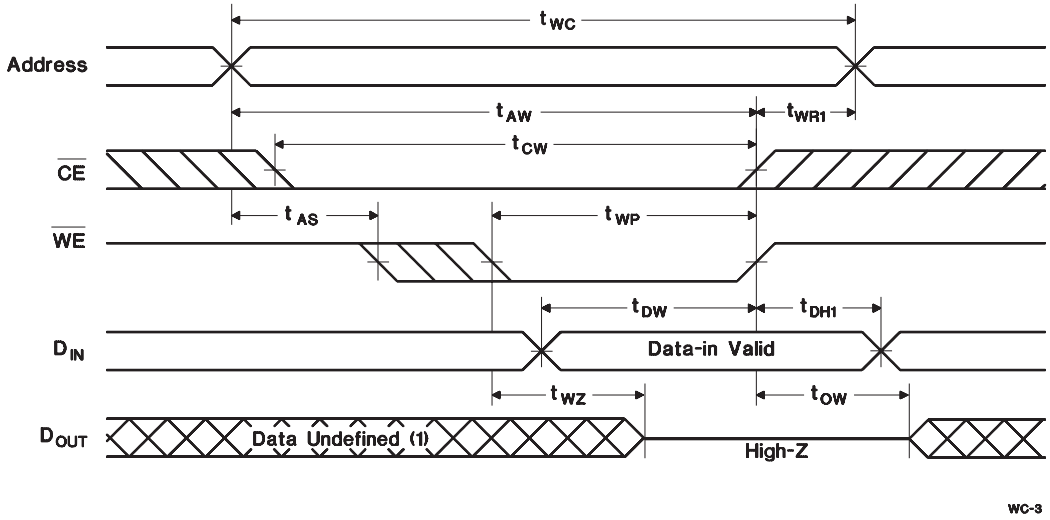
Symbol	Parameter	-70		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	70	-	ns	
t_{CW}	Chip enable to end of write	65	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	ns	(1)
t_{AS}	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	ns	I/O pins are in output state. (5)

Notes:

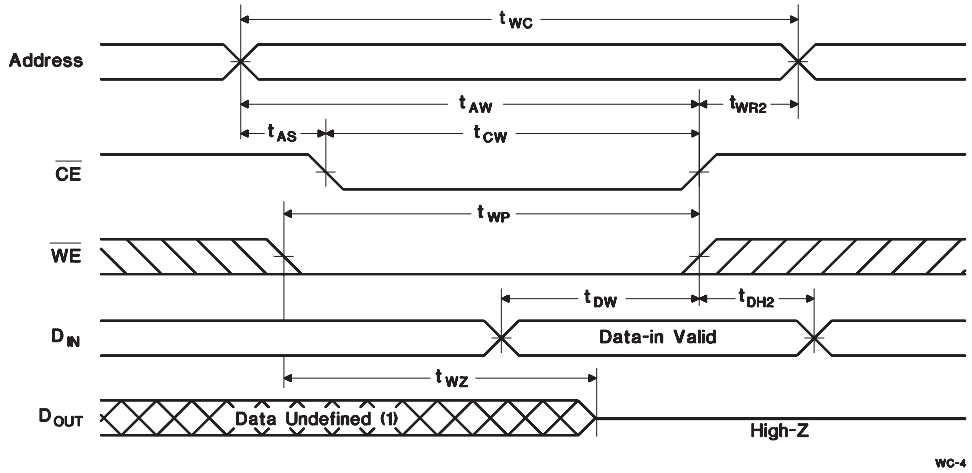
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Not Recommended for new Designs

Write Cycle No. 1 (WE-Controlled) [1,2,3]



Write Cycle No. 2 (CE-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Not Recommended for new Designs

Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

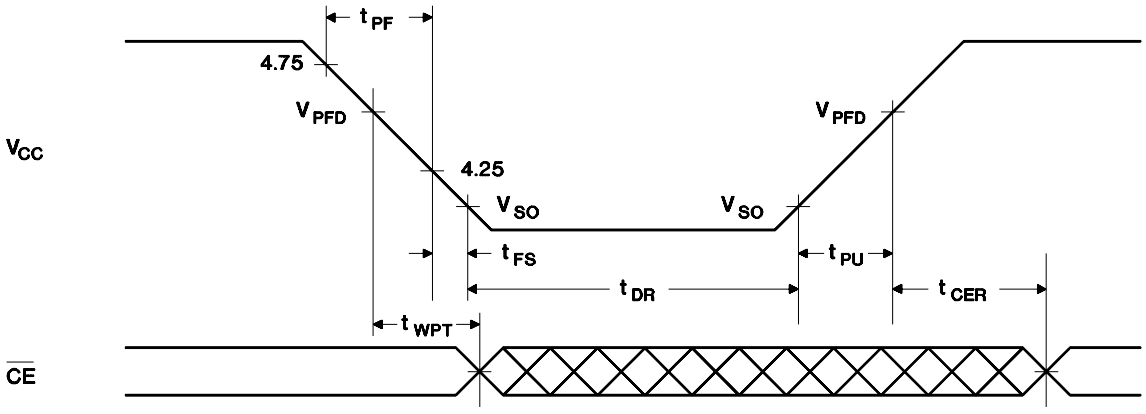
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	5	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

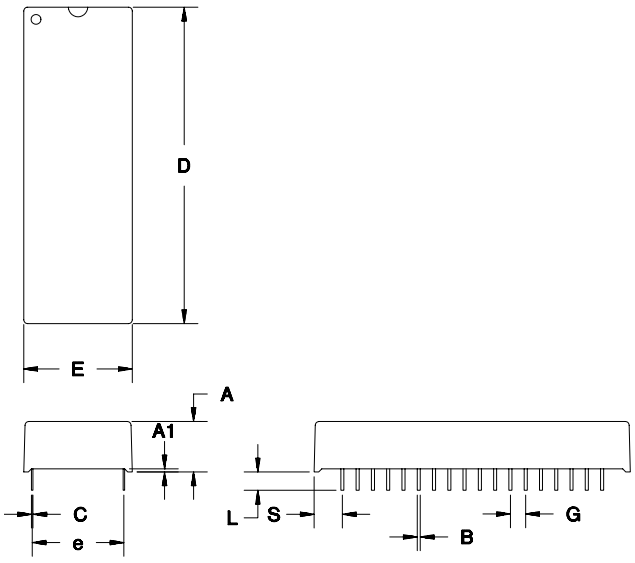
Power-Down/Power-Up Timing



PD-B

Not Recommended for new Designs

MC: 36-Pin C-Type Module



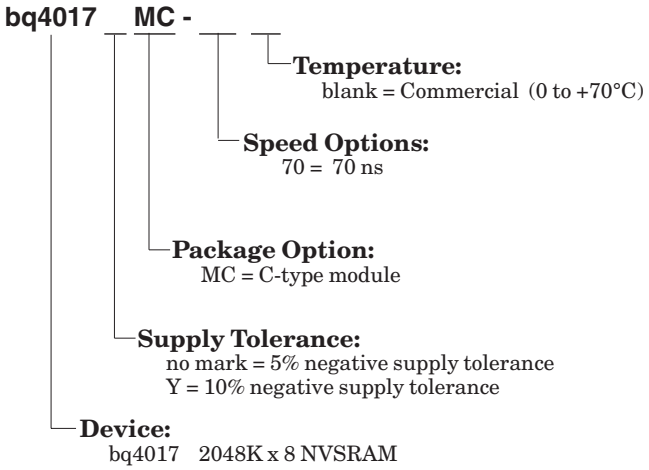
36-Pin MC (C-Type Module)

Dimension	Minimum	Maximum
A	0.365	0.375
A1	0.015	-
B	0.017	0.023
C	0.008	0.013
D	2.070	2.100
E	0.710	0.740
e	0.590	0.630
G	0.090	0.110
L	0.120	0.150
S	0.175	0.210

All dimensions are in inches.

Not Recommended for new Designs

Ordering Information



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ4017MC-70	OBSOLETE	DIP MODULE	MC	36		TBD	Call TI	Call TI	0 to 70		
BQ4017YMC-70	OBSOLETE	DIP MODULE	MC	36		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

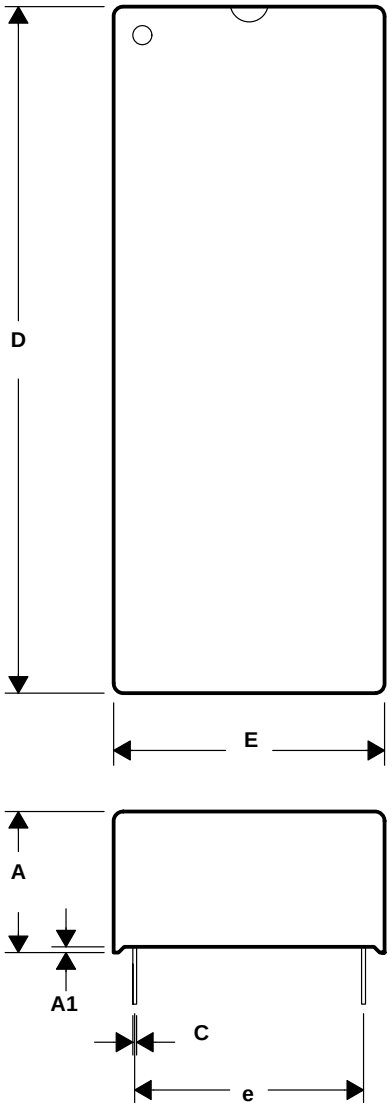
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MPDI063 – MAY 2001

MC (R-PDIP-T36) **PLASTIC DUAL-IN-LINE**



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	–	0.38	–
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.175	0.210	4.45	5.33

4201977/A 03/01

NOTES: A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated